

In the Claims:

Please amend the claims as follows.

1. (*Currently amended*) A test access architecture for testing a cascade of modules embedded in an electronic circuit, each of the modules being isolated from surrounding circuitry by an associated test wrapper that provides switching functionality between functional access and test access to its associated module, the test access architecture comprising:

a test access mechanism arranged to transport test stimulus data ~~and test response data to and from~~ a module of the cascade that is in a test mode being tested and to transport test response data from the module in the test mode, respectively, the test access mechanism configured to transport the test stimulus data and the test response data via a single data path that passes through each module of the cascade;

circuitry configured to provide a global enable signal that is provided to each of the modules, the global enable signal provided for placing the modules in the [[a]] test mode; and

a plurality of control circuits, each of the control circuits ~~provided between the global enable signal and an~~ associated with one of the modules and each of the control circuits arranged to control whether or not the global enable signal is passed to its associated module.

2. (*Currently amended*) The test access architecture as recited in claim 1, wherein each module of the cascade is configured to operate in one of two modes, each of the modes using the single data path, the first mode being a transport mode in which the test stimulus and response data is passed through the module unmodified and the second mode being the test mode in which the module generates the test response data from the test stimulus data, and wherein each of the control circuits is controlled by a dedicated bypass signal for its associated module.

3. (*Previously presented*) The test access architecture as recited in claim 2, wherein each of the control circuits is connected to receive the global enable signal and the dedicated

bypass signal, and each of the control circuits is arranged to provide a local enable signal to its associated module based on the respective states of the global enable signal and the dedicated bypass signal.

4. *(Previously presented)* The test access architecture as recited in claim 3, wherein each of the control circuits is arranged to pass the global enable signal if its associated module is being tested, and to block the global enable signal if its associated module is not being tested.

5. *(Currently amended)* The test access architecture as recited in claim 1, wherein the test access mechanism is configured to simultaneously transport multiple sets of test stimulus data to the module being test via the single data path, and wherein each of the control circuits is an OR gate.

6. *(Previously presented)* The test architecture as recited in claim 1, wherein each of the control circuits is an AND gate.

7. *(Currently amended)* The test architecture as recited in claim 1, wherein the test access mechanism is configured to place the modules of the cascade that are not being tested in a transport mode of operation in which the modules not being tested do not modify the test stimulus data being transported to the module in the test mode and the modules not being tested do not modify the test response data being transferred from the module in the test mode, and wherein the electronic circuit is an integrated circuit.

8. *(Currently amended)* The test architecture as recited in claim 7, wherein each of the control circuits is located within the [[a]] test wrapper of its associated module.

9. *(Previously presented)* The test architecture as recited in claim 7, wherein each of the control circuits is located in a test control block of a system on chip.

10. (*Currently amended*) The test architecture as recited in claim 1, wherein the test access mechanism is arranged to load the test stimulus data into the module in the test mode being tested from another one of the modules in a pipelined manner and to unload the test response data from the module in the test mode being testing into a further one of the modules in a pipelined manner.

11. (*Currently amended*) The test architecture as recited in claim 1, wherein the global enable signal is global to the test access mechanism (TAM), and wherein the plurality of modules are connected to the TAM, the TAM configured to place the other modules in a transport mode of operation while the module is in the test mode.

12. (*Previously Presented*) The test architecture as recited in claim 1, wherein the global enable signal is global to more than one test access mechanism (TAM) on the electronic circuit.

13. (*Currently amended*) A method of testing a module in an electronic circuit, the module being one of a cascade plurality of modules embedded in the electronic circuit, the cascade of modules being connected in series to a test access mechanism (TAM), each of the modules being isolated from surrounding circuitry by an associated test wrapper that provides switching functionality between functional access and test access to its associated module, the test access mechanism arranged to transport test stimulus data to the [[a]] module being tested, and to transport test response data from the module being tested, the test access mechanism configured to transport the test stimulus data and test response data via a single data path that passes through each module of the cascade, the method comprising the steps of:

- loading a first set of test stimulus data into the module being tested;
- testing the module in response to a global enable signal being activated;
- unloading test response data captured from the module being tested; and
- during the testing step, placing the other modules connected to the test access mechanism (TAM) in a transport mode of operation, wherein, in the transport mode of operation, the other modules do not corrupt a second set of test stimulus data being

loaded into the module being tested, and the other modules do not corrupt previous test response data being unloaded from the module being tested.

14. (*Previously presented*) The method as recited in claim 13, further comprising the step of providing a plurality of control circuits, each of the control circuits located between the global enable signal and an associated one of the modules, wherein each of the control circuits is arranged to control whether or not the global enable signal is passed to its associated module.

15. (*Previously presented*) The method as recited in claim 14, wherein each of the control circuits is controlled by a dedicated bypass signal.

16. (*Previously presented*) The method as recited in claim 15, wherein each of the control circuits is connected to receive the global enable signal and the dedicated bypass signal, and each of the control circuits is arranged to provide a local enable signal to its associated module based on the respective states of the global enable signal and the dedicated bypass signal.

17. (*Previously presented*) The method as recited in claim 16, wherein each of the control circuits is arranged to pass the global enable signal if its associated module is being tested, and to block the global enable signal if its associated module is to be placed in the transport mode.

18. (*Previously presented*) The method as recited in claim 14, further comprising the step of providing an OR logic function as each of the control circuits.

19. (*Previously presented*) The method as recited in claim 14, further comprising the step of providing an AND logic function as each of the control circuits.

20. (*Previously presented*) The method as recited in claim 14, further comprising the step of providing each of the control circuits within a test wrapper of its associated module.

21. *(Previously presented)* The method as recited in claim 14, further comprising the step of providing each of the control circuits in a test control block of a system on chip.

22. *(Previously presented)* The method as recited in claim 15, further comprising the step of providing each of the control circuits within its associated module.

23. *(Previously presented)* The method as recited in claim 13, wherein the test pattern data is processed in a pipelined manner in which ones of the modules located prior to the module being tested contain further sets of test stimulus data from a series of test stimulus data, and ones of the modules located after the module being tested contain test response data from previous tests.

24. *(Currently amended)* The method as recited in claim 13, wherein the first set of test stimulus data is loaded into the module being tested from another one of the modules and the test response data captured from the module being tested is unloaded into a further one of the modules, and wherein the global enable signal is arranged to be global to the test access mechanism (TAM).

25. *(Previously Presented)* The method as recited in claim 13, wherein the global enable signal is arranged to be global to more than one test access mechanism (TAM) on the electronic circuit.